A Novel MMIC Power Amplifier for Pocket-Size Cellular Telephones

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Abstract - A novel MMIC power amplifier for cellular telephones is proposed. The amplifier which is named UBIC-PA (Unbalanced Bias Cascode Power Amplifier) enables making very compact monolithic integration in spite of the considerably low frequency of 900 MHz-band. The MMIC UBIC-PA has more than 40 dB gain, 29 dBm output power and 62% power added efficiency at the supplied voltage of 6V. The chip size of the MMIC without an output matching circuit is 2.4 x 2.4 mm. The size and cost of the UBIC-PA module is estimated at about 1/6 (0.2 cc) and 1/2 that of the former hybrid PA module. Moreover, the UBIC-PA improves power dissipation by more than 50% under medium and low output power conditions. This is very important for cellular telephones employing adaptive transmitter power control for battery saving.

I. Introduction

Recent growth in the cellular telephone market has been accelerated by the appearance of Motorola's Micro-TAC throughout the world. R & D activities in Japan are concentrating on developing smaller size cellular telephones with reasonable cost.

The battery size is the main obstacle in reducing the size of cellular telephones. A power amplifier (PA) decides the battery size because the PA consumes the greater part of the power. Therefore, it is very important to increase the efficiency of the PA as well as to reduce the size of the PA. Moreover, cellular systems employ adaptive transmitter power control for battery saving and the transmitter power is frequently controlled at medium and low output power. Therefore, PAs are required to maintain high efficiency under medium and low output power conditions as well as high power conditions. In addition, reducing the cost of the PAs is another important subject since the PAs are one of the highest cost components of cellular telephones.

This paper describes a novel MMIC power amplifier for cellular telephones. The amplifier which is named the UBIC-PA (Unbalanced Bias Cascode Power Amplifier) enables making very compact monolithic integration in spite of the considerably low frequency of 900 MHz-band. Designing compact monolithic power amplifiers in frequencies of less than 1 GHz is more difficult than that of higher frequencies because matching circuits with low loss and high current capacity requires long and wide conductor lines, which results in larger PAs. The MMIC UBIC-PA has more than 40 dB gain, 29 dBm output power and 62% efficiency at the supplied voltage of 6V. The chip size of the MMIC without an output matching circuit is 2.4 x 2.4 mm. The GaAs MMIC chip area is only twice the total GaAs FET chip area of a hybrid 4-stage power amplifier with the same gain and power. The cost of the MMIC UBIC-PA is lower than that of hybrid-IC PAs because of low assembling and testing cost. The size and cost of UBIC-PA module is estimated at about 1/6 (0.2 cc) and 1/2 that of the former hybrid PA module for cellular telephones.

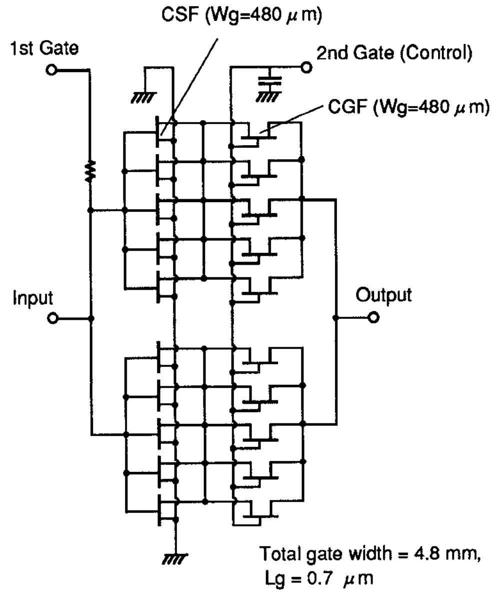

Fig. 1. Configuration of power UBIC-FET.

II. Features of the proposed UBIC-FET (Unbalanced Bias Cascode FET)

The power UBIC-FET employs a parallel connection of cascode circuits [1],[2] of a common source FET (CSF) and a common gate FET (CGF) as shown in Fig. 1. Here, the drain terminal of the CSF and the source terminal of the CGF are directly connected and no circuit element is connected between them. Figure 2 shows the input power versus the output power and the power added efficiency (PAE) of the UBIC-FET compared with a conventional CSF. The UBIC-FET achieves a linear gain of 26 dB which is 10 dB higher than that of the CSF with the same gate length (0.7 μm) and total gate periphery (4.8mm). The PAE of the UBIC-FET is comparable to that of the CSF and the input power at the maximum PAE for the UBIC-FET is 10 dB lower than that for the CSF. This implies that the UBIC-FET can reduce the number of power amplifier stages for cellular telephones with no degradation in the efficiency. Moreover, the UBIC-FET provides easy and direct output power control by using the the second gate. Figure 3 shows the control voltage dependency of the output power and the PAE. As shown in Fig.3, the optimal control voltage for high-power and high-efficiency is around 0.9V. Figure 4 shows the allotment of supplied voltage between the CSF and the CGF in the UBIC-FET at the external supplied voltage of 6V. To achieve high power and high efficiency, the greater part of the supplied voltage should be applied to the CGF. This is the reason the output power is decided only by the supplied voltage and current to the CGF and the supplied voltage to the CSF does not contribute to the output power. Moreover, the supplied voltage of 1V is enough for the CSF because the CSF does not require the output power, but the gain. This condition is realized by setting a low control voltage at the 2nd gate. The allotment of supplied voltage between the CSF and the CGF for high power and high efficiency is very different from that of ordinary cascode FETs for a small-signal high-gain condition. Therefore, we call this cascode FET, the UBIC-FET (Unbalanced Bias Cascode FET). Why does the UBIC-FET provide such a high efficiency in spite of the handicap in the series FET configuration? This comes from the definition of the power added efficiency. The power added efficiency is derived from the following equation.

$$PAE = \frac{Pout - Pin}{Vd \cdot Id} = \frac{Pin\,(G - 1)}{(V_{CGF} + V_{CSF})\ Id}$$

Where, Pout, Pin, Vd, Id, VCGF, VCSF and G are RF output power, RF input power, supplied drain voltage, supplied drain current, supplied voltage to the CGF, supplied voltage to the CSF and power gain, respectively. While the UBIC-FET has a disadvantage in output power because the supplied drain voltage to the CSF does not contribute to the output power, it has an advantage of low input power because of the additional gain of the CSF. This fact results in providing comparable efficiency to a conventional CSF as shown in Fig. 2.

Figure 5 shows the measured PAE versus output power under several control voltages. The maximum PAE curve to the desired output power is derived by changing the control voltage and input power. The efficiency over the wide output power range is effectively increased by changing the control voltage and input power of the UBIC-FET as shown in Fig.5.

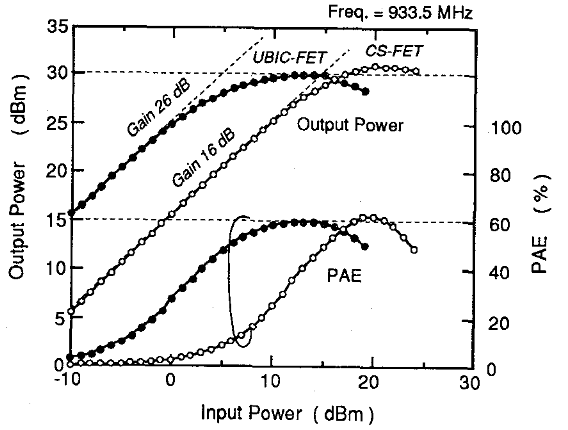

Fig. 2. Output power and PAE versus input power of UBIC-FET and CS-FET.

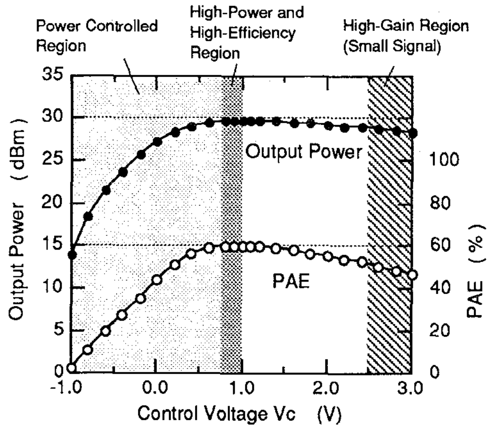

Fig. 3. Control voltage dependency of the output power and PAE of the UBIC-FET.

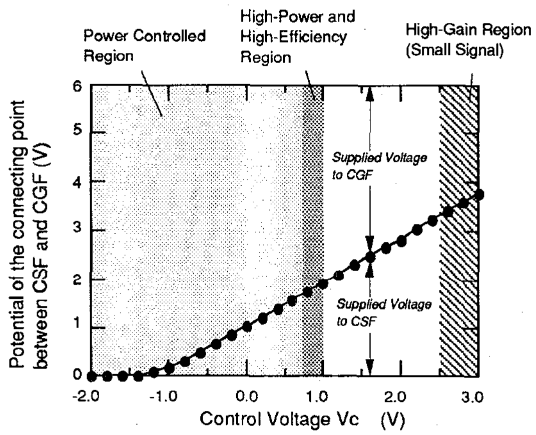

Fig. 4. Allotment of the supplied voltage between the CSF and CGF in the UBIC-FET.

III. UBIC-PA design

Figure 6 shows a schematic diagram of the UBIC-PA with an automatic output power control. The PAs for cellular telephones in the NTT system require more than a 40 dB gain and 20 dB output power control with five operation power levels (4 dB step). A conventional PA employs a 4-stage configuration of CSFs and the power control is made by changing the drain voltage and current for the pre-amplifiers. On the other hand, the proposed UBIC-PA employs a 2-stage configuration using UBIC-FETs and the power control is done by changing the control voltage of both UBIC-FETs. The monolithic integration is applied to the greater part of the PA with the exception of the output circuit because the elimination of the inter-stage matching circuits and bias circuits provides compact layout of integration. A prototype power amplifier module, shown in Fig. 7, consisting of a MMIC chip and a hybrid output circuit has been fabricated and tested to demonstrate the UBIC-PA features.

IV. Measured Performance

Figure 8 shows the input power versus the output power and PAE of the UBIC-PA. The PA achieves more than 62% PAE with 40 dB gain and 29 dBm output power at a drain voltage of 6V. Moreover, the UBIC PA had more than 60% PAE at a drain voltage of more than 3V. This indicates the UBIC PA has no serious disadvantage in the low voltage operation in spite of the series FET configuration.

Figure 9 shows the PAE versus the relative output power level of the UBIC-PA and a conventional PA. The UBIC-PA can improve the PAE because it saves power consumption in the medium and low output power range by changing the control voltage. The PAE in the case of the dual control for the 1st and 2nd UBIC-AMPs, according to Fig. 5, is higher than that in the single control for the 2nd UBIC-AMP. The reduction in power consumption in the medium and low output power range is very important for cellular telephones employing adaptive transmitter power control for battery saving. This is because the PA for cellular telephones is frequently controlled to medium and low output power levels.

V. Conclusion

A new power amplifier for pocket-size cellular telephones has been presented and described. The UBIC-AMP configuration provides compact monolithic integration and high efficiency over a wide output power level. The size and cost of UBIC-PA module is estimated at about 1/6 (0.2 cc) and 1/2 that of the former PA module for cellular telephones. Therefore, we believe the UBIC-PA will highly contribute to the next generation of cellular telephones.

Acknowledgment

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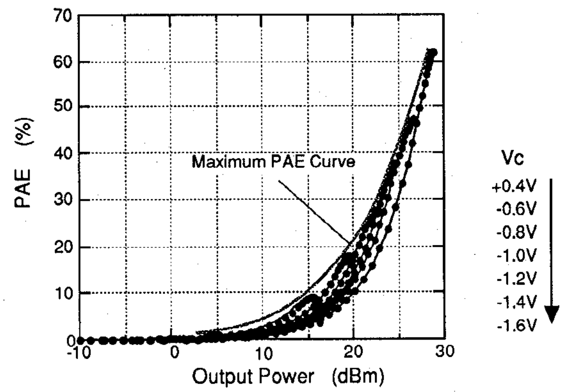


Fig. 5. Measured PAE versus output power under several control voltages.

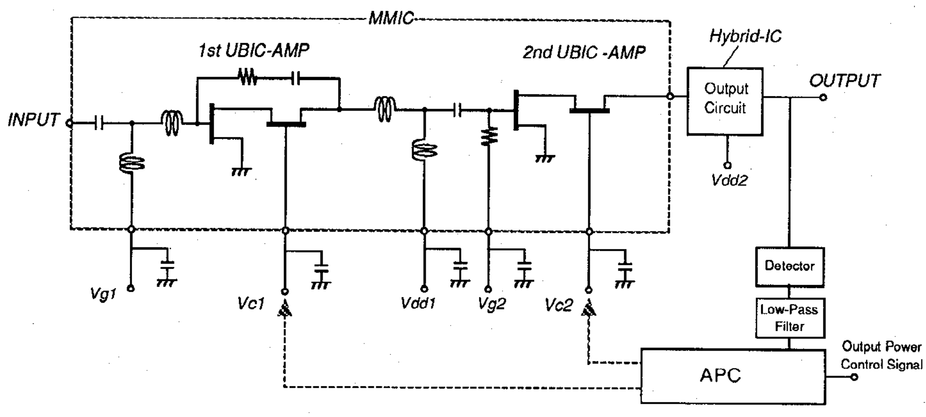


Fig. 6. Schematic diagram of the UBIC-PA with automatic output power control.

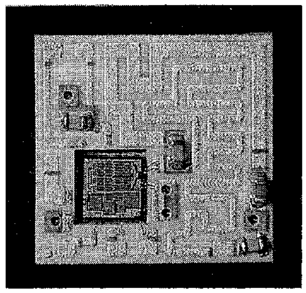
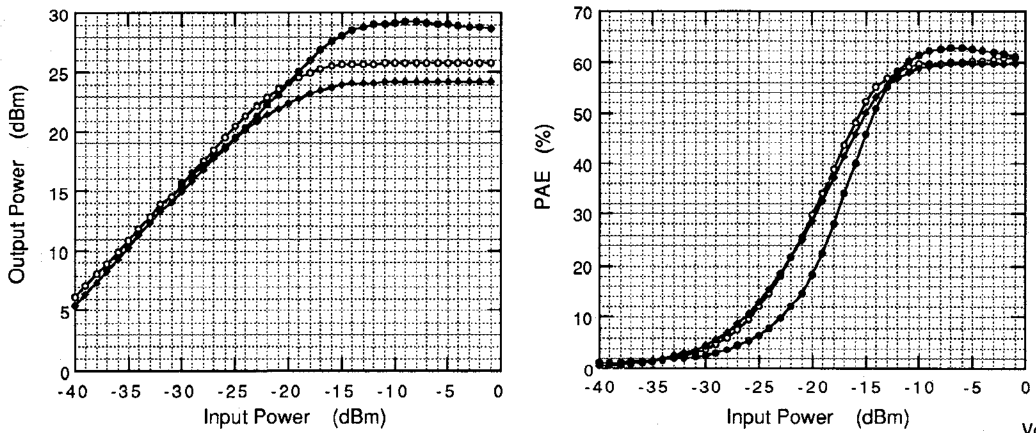


Fig. 7. Prototype UBIC PA module.
Module size : 9 x 9 x 2.5 mm (0.2cc)
GaAs MMIC size : 2.4 x 2.4 mm.



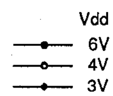


Fig. 8. Input power dependency of output power and PAE for UBIC-PA.

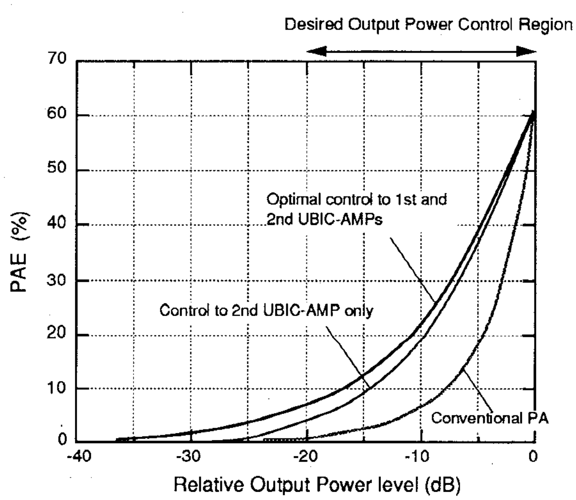


Fig. 9. PAE versus relative output power level
of UBIC-PA and conventional PA.